What is claimed is:

1. A ferroelectric memory device, comprising:

a memory cell unit having hierarchical bit-line structure formed by forming a word line and a plate line in a direction of a row and forming sub-bit line and main bit line in a direction of crossing the word line and the plate line, and including a plural memory cells equipping a ferroelectric capacitor coupled to the sub bit line and a first current gain transistor having a gate coupled to the sub bit line, one end connected to a ground, and other end connected to the main bit line;

a reference cell unit having hierarchical bit line structure formed by forming a reference word line and reference plate line in a direction of a row and forming a reference sub bit line and a reference main bit line in a direction of crossing the reference word line and reference plate line, and including a reference cell quipping a ferroelectric capacitor coupled to the reference sub bit line and a second current gain transistor having a gate connected to the reference sub bit line, an one end connected to a ground power supplying end and another end connected to the reference main bit line; and

a sense amp unit for comparing voltages of the main bit line of the memory cell unit and the reference main bit line of the reference cell unit, amplifying the voltage difference and outputting data,

wherein a size of the two ferroelectric capacitor in the memory cell and the reference cell is identical and a size of the first current gain transistor and the second current gain transistor is different.

2. The ferroelectric memory device as recited in claim 1, wherein the ferroelectric capacitor of the reference cell generates a reference voltage by using non-switching charge, the first and second current gain transistor are NMOS transistors, and a width of the second current gain transistor is wider comparing to the first current gain transistor.

3. The ferroelectric memory device as recited in claim 1, wherein the ferroelectric capacitor of the reference cell generates a reference voltage by using switching charge, the first and second current gain transistor are NMOS and a length of the second current gain transistor is longer comparing to the first current gain transistor.

4. The ferroelectric memory device as recited in claim 1, wherein the memory cell unit further includes a first load transistor having a gate connected to a ground, one end connected to the main bit line, and other end connected to the power supplier, and the reference cell unit further includes a second load transistor having a gate connected to the ground, one end connected to the reference main bit, and other end connected to the power supplier.